**Micromachining Final Lab Report**

**Aidan Mulligan**

**Friday 9 am Lab Session - Vincent Banh**

## Abstract

In our micromachining lab, we fabricated a conductivity-measuring device to be used by the Porter Lab at BYU for research into lithium-ion batteries. We had to deposit and pattern platinum metal on our wafers, insulate the metal with deposited $SiO_2$, dice and solder the wafers, and then test the effectiveness of the resulting devices. These steps required us to perform processes including lithography, etching, lift-off, PECVD, sputtering, laser etching, and other micromachining techniques. When we performed these techniques, our lab section was quite successful as most of the wafers were fabricated successfully. The most notable error occurred in the photolithography step for patterning the platinum metal, as a mistake in the mask resulted in an electrical short on one side of each wafer. The other side of each wafer was still functional, and the rest of the processes continued effectively. When the final devices were tested, they were found to be effective at measuring the conductivity of a solution.

## 1. Introduction

In this lab, we fabricated a chip that will be used by the Porter Lab at BYU to study lithium-ion batteries. The purpose of the chip is to measure the conductivity of between a substrate and a modified flow cell using platinum electrodes. Studying battery electrolytes is important because different electrolyte solutions possess different properties, and by studying them we may design longer-lasting and more powerful batteries. Four-electrode conductivity measurements are important because a four-electrode measurement allows for very accurate measurements of the resistance of a solution, which makes a four-electrode device optimal for conductivity measurements (as seen in Figure 1).

The devices were manufactured using micromachining processes that are outlined in Figure 2. The glass wafer was first patterned with platinum metal, which involved photolithography, sputtering, and lift-off. Afterwards, $SiO_2$ was patterned over the device to insulate areas of the metal: this involved photolithography, and $SiO_2$ etching steps. Then, holes were laser-etched through the wafer, it was diced, and it was soldered. The final device was then tested. The outcome of the chips in my section were very positive.

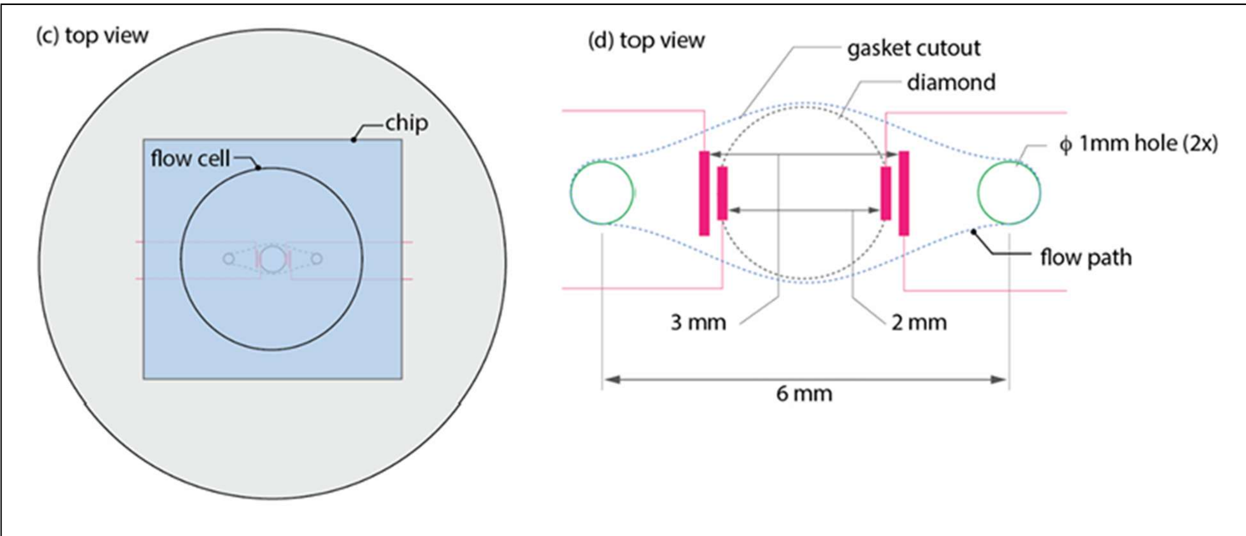



**Figure 1 (courtesy of Prof. Jason Porter):** This figure shows the design of the final device that will be used by the Porter Lab.

Photoresist Platinum $SiO_2$

**Process flow (cross section through electrodes):**

**Lab:**

1. Borosilicate glass wafer
2. Photolithography
3. Sputtering
4. Photoresist removal
5. PECVD $SiO_2$
6. Photolithography
7. $SiO_2$ etch
8. Laser etching
9. Soldering
10. Testing

"Lift-off" (steps 2–4)

flow cell
chip

**Figure 3:** Lab process flow.

**Figure 2:**
This figure shows the process flow of the lab, from an initial glass wafer to a working device.

## 2. Methods

### 2.1 Overview and Mask Design

The silicon wafers used in this lab were made of Glass Borofloat33 material, with a diameter of 100 ± 0.1 mm, a thickness of 0.7 ± 0.025 mm, and a surface arithmetic average roughness (Ra) of < 1 nm. Lithography was performed in a class 100 cleanroom. All other steps were performed in a class 1000 cleanroom with the exception of chip assembly and chip testing, which were performed in the prototype lab and Professor Warren's lab respectively. Two photolithography masks (for metal and $SiO_2$ patterning) were designed in AutoCAD and patterned by a Heidelberg MicroPG (μPG) 101 using a 405 nm laser with a resolution of 5 μm.

### 2.2 Metal Patterning (Lift-Off)

Wafers were cleaned using a PE II-A plasma cleaning machine with oxygen for 1 minute at 200 W. Wafers were then spin-coated by a CEE Apogee spin coater for 45 seconds at 2000 rpm, depositing a layer of xylene (20:80%). The same parameters were then used to spin coat S1813 photoresist onto the wafer. Afterwards, wafers were soft-baked by a SN 780 machine for 1 minute at 110°C. Proximity printing photolithography was then performed on the wafers using the EV 420 machine with a wavelength between 350 to 450 nm. Wafers were then immersed in AZ 1:1 developer for 2 minutes, rinsed with water, dried with nitrogen, and baked again for 1 minute at 110°C.

Next, we used a Denton 653 sputtering machine to sputter a target thickness of 10 nm of chromium and 50 nm of platinum onto the top of each wafer. The chromium was deposited over 2.5 minutes using 50 W of DC1 power, while the platinum was deposited over 8.7 minutes using 50 W of DC1 power.

Next, lift-off was performed to remove photoresist and unwanted metal. Each wafer was sonicated inside a tank filled with acetone solvent. The time for sonication varied from 15 to 23 minutes, dependent on the wafer. Wafers were cleaned with acetone, IPA, and DI $H_2O$ before being dried with Nitrogen air.

### 2.3 Oxide Patterning

Before PECVD, we cleaned each wafer in a PE II-A wafer cleaner (as described in section 2.2 above). We Then performed PECVD using an Oxford Instruments Plasmapro 100 Cobra 300 dry etching system, aiming to deposit a 250 nm layer of $SiO_2$. Deposition was performed for 42 minutes at 1400 Watts of power, using the gases $N_2O$ and $SiH_4$ at a ratio of 90 to 38.3.

Spin-coating and baking were performed again (as described above in section 2.2). Photolithography was repeated using a different mask in the EV 420 machine (as described above in section 2.2). The development steps were the same as before (see section 2.2).

Next, oxide etching was performed by immersing wafers for 3 minutes in a 6:1 BOE etchant, rinsing them in an $H_2O$ bath for at least 1 minute, and then drying them off with $N_2$ gas. Wafers were then rinsed thoroughly in acetone to strip off any remaining photoresist, before being rinsed again with di H2O and dried with $N_2$ gas

## 2.4 Chip Assembly

Next, four holes were laser-etched through the wafer using a Universal Laser Systems PLS6.150D laser cutter running Coreldraw software. Once aligned, wafers were taped down and etched from the back of the wafer to avoid scratches on the front. Cutting runs were repeated 12 times per wafer, using only yellow and magenta layers at 50% power, 10% speed, and 1000 pixels per inch. Waste glass was removed with a razorblade.

Before dicing, we applied a protective layer of tape across each wafer. Next, we diced the wafers using a Disco DAD641 Automatic Dicing Saw, which we had calibrated. We utilized a 58 mm diameter and 0.15 mm thick saw blade and set the machine to 10% sensitivity after cleaning with ethanol. A single cut was made in the center of each wafer using a feed speed of 1.500 mm/s and a spindle revolution of 30000 rpm, splitting each wafer into two halves.

Wires were then soldered onto the soldering pads (4 per half and 8 per wafer) of each wafer. The small wires were stripped, and flux was applied to the soldering pads, before the wires were soldered to the pads using a soldering iron inside a vented hood.

## 2.5 Characterization and Testing

Optical microscopy was performed to make images of the device microstructure and profilometry to measure thickness. Profilometry was performed using a Tencor P-10 surface profilometer for most measurements and a Tencor P-20H profilometer after sputtering. Although we planned to use a Nanospec 3000 reflectance spectrometer after PECVD, there were issues with the instrument and we resorted to profilometry instead.

Once the devices were machined, they were tested using an Interface 1000E Potentiostat manufactured by Gamry Instruments. A four-electrode measurement was performed for each device at 3 different concentrations of NaCl solution: 1.0 g/L, 3.0 g/L, and 6.0 g/L. We set the device to use an AC voltage of 10 mV and measure frequencies ranging from an initial frequency of $2*10^6$ to a final frequency of 1 Hz.

**3. Results & Discussion**

The overall lab process for our section went very smoothly and was quite efficient. Most of the original wafers ended up as functional devices by the end of the process. The most notable error that occurred was an electrical short caused by an issue with the lithography mask in the metal patterning step. In the sections below, the results of each process step are discussed as they relate to the machining of these devices.

<u>3.1 Mask Design</u>

Two different patterns were used as masks for the metal patterning and $SiO_2$ patterning steps, respectively. Pictures of these two masks are visible in Figure 3. A clear field mask (Figure 3a) was used for metal patterning with a positive photoresist while a dark field mask (Figure 3b) was used for oxide patterning by a negative photoresist.

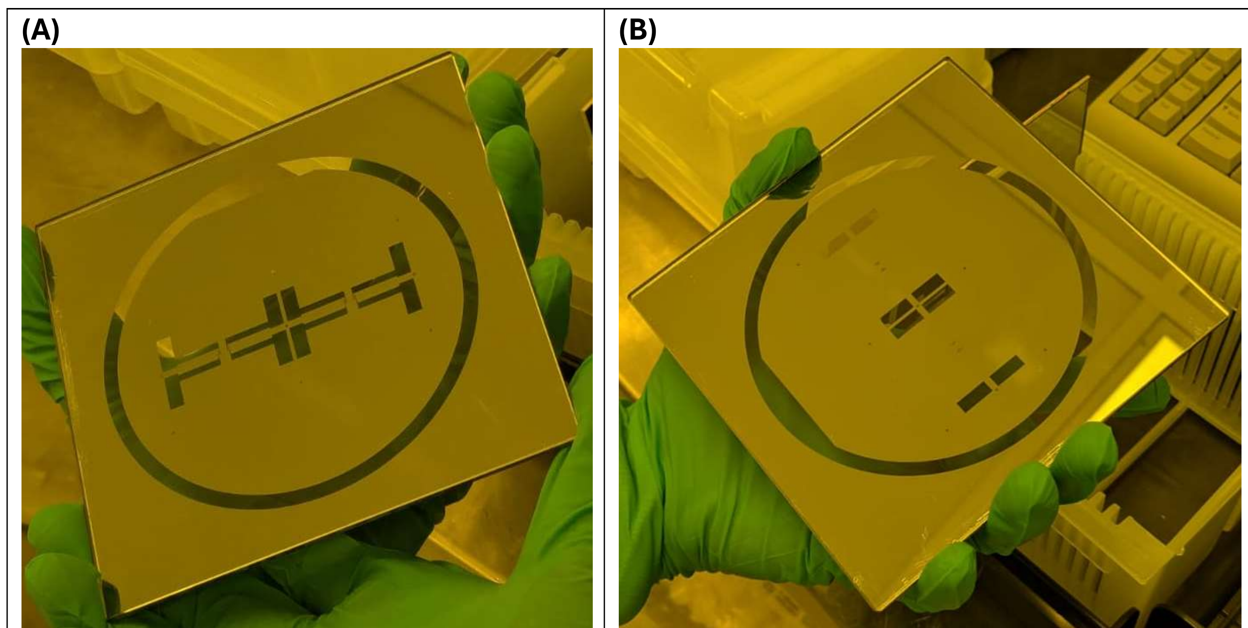



**Figure 3:** These pictures show the two lithography masks. (A) is a clear field mask that patterned the metal while (B) is a dark field mask that patterned the $SiO_2$ insulation layer

3.2 Metal Patterning

The full metal patterning process turned out good for wafers in our lab section. The only issue was that a short became visible on one side of each wafer following the lift-off process, and we believe that this short was caused by an issue in the lithography mask.

The lithography step was completed efficiently. After development, we some data. Both the photograph (Figure 4) and microscope image (Figure 5) show that the developed features on the wafer are very well-defined, which is good. Because the Nanospec 3000 was having technical issues, we used a Tencor P-10 profilometer to measure the photoresist thickness. The profilometer measured a thickness of 1.647 μm, which is reasonable for our device.

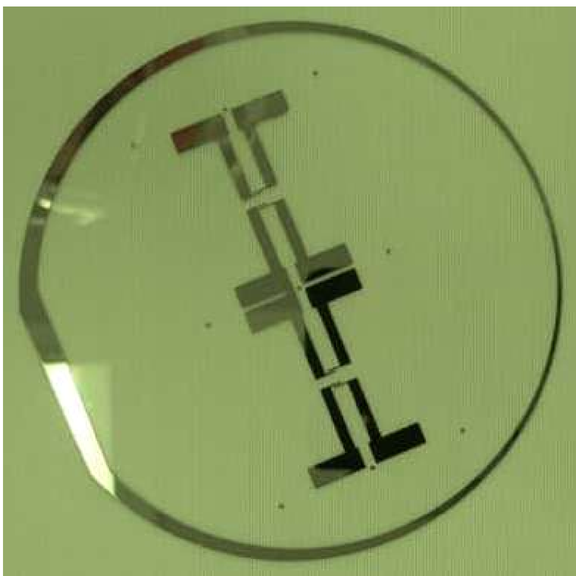
The sputtering steps went exactly to plan, depositing a smooth layer that can be seen in the photo (Figure 6). Using a profilometer and a glass slide, we measured the thickness of the combined platinum and chromium layers to be 59 nm thick. This result is very close to the target thickness of 60 nm (10 nm of Cr, 50 nm of Pt).

The liftoff step also went effectively. The sonication times ranged from 15 minutes to 23 minutes, depending on the wafer. The wafer was clearly patterned following liftoff, as can be seen in a photograph (Figure 7) and microscope image (Figure 8). The feature size was around 16.99 μm to 17.47 μm, as seen in Figure 8.

**Figure 4:** The features are clearly visible in this photograph of the photoresist pattern following development.

| | |
|---|---|
| | **Figure 5:** In this microscope image of the developed photoresist pattern, the features turned out well. |

| | |
|---|---|
| | **Figure 6:** sputtering deposition leaves a thin and smooth layer of Pt coating the surface. |

| | |
|---|---|
|  | **Figure 7:** The final pattern came out well for the wafers. The only issue is that there is an electrical short visible in the center of the wafers, which seems to be a mask-related issue. |

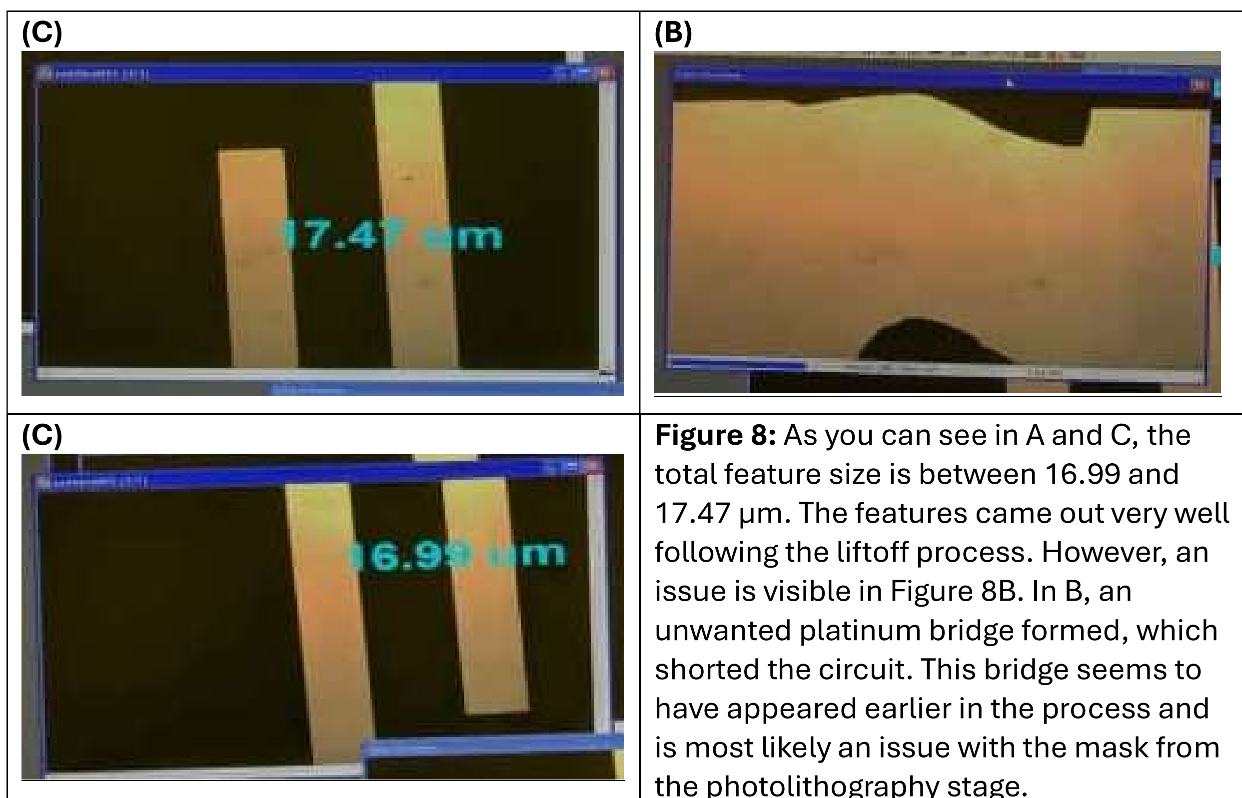



**Figure 8:** As you can see in A and C, the total feature size is between 16.99 and 17.47 µm. The features came out very well following the liftoff process. However, an issue is visible in Figure 8B. In B, an unwanted platinum bridge formed, which shorted the circuit. This bridge seems to have appeared earlier in the process and is most likely an issue with the mask from the photolithography stage.

### 3.3 Oxide Patterning

Unlike the metal-patterning stage where an electrical short became visible, there were no major problems with the $SiO_2$ patterning stage. The most notable occurrence was a delay caused by hardened photoresist on the mask, which was sorted out.

The wafers had a tinted red color following a successful PECVD (Figure 9). The thickness achieved was close to the 250 nm target: in one wafer the average thickness was 242.42 nm whereas it was 250.76 nm in another wafer (Table 2). Measurements were consistent, with the wafers a standard deviation of 0.998 nm and 3.549 nm, respectively. This indicates that while there was variability between wafers, the deposited layers were smooth. Possible reasons that one wafer had a lower-than-expected thickness include lower pressure, limited gas flow, or low power.

Although some wafers were slightly misaligned, the wafers were operable following photolithography. In Figure 10 the photoresist is closely aligned with the features from the previous metal patterning stage, and the measured width of the feature was 16.73 µm. Additionally, profilometry readings showed that the height of the photoresist was 1.505 µm

above the wafer, which is good for our project. One thing to note is that the mask was scratched and covered in hardened photoresist by a previous group. Before running the photolithography, we soaked the mask in isopropanol and acetone to clean it. Although this put our group behind, it did not end up having an effect on the photolithography results.

Chemical etching was successful, as can be seen in Figure 11 below where the color of the wafers was darker following the step. The probes and soldering pads were both 0.234 μm in thickness (Table 3), according to a profilometer measurement that can be seen in Figure 11. This suggests a uniform thickness, which is desirable.

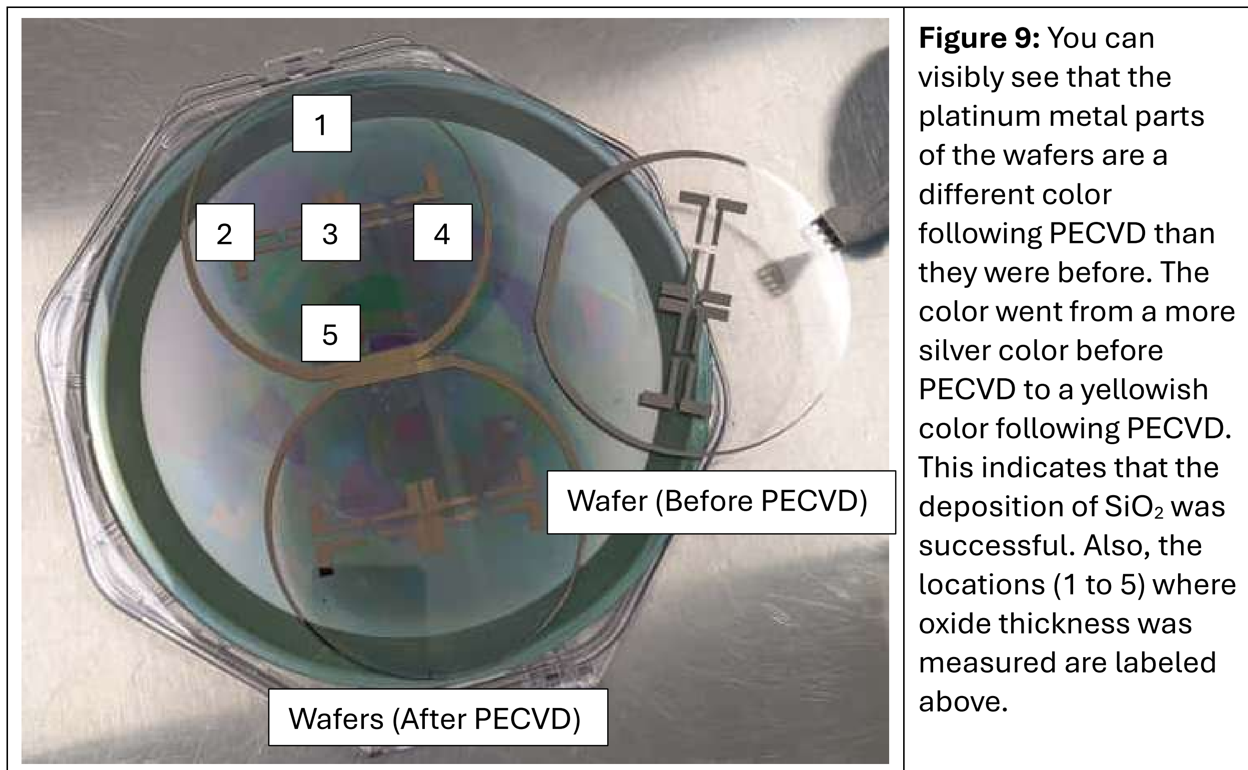
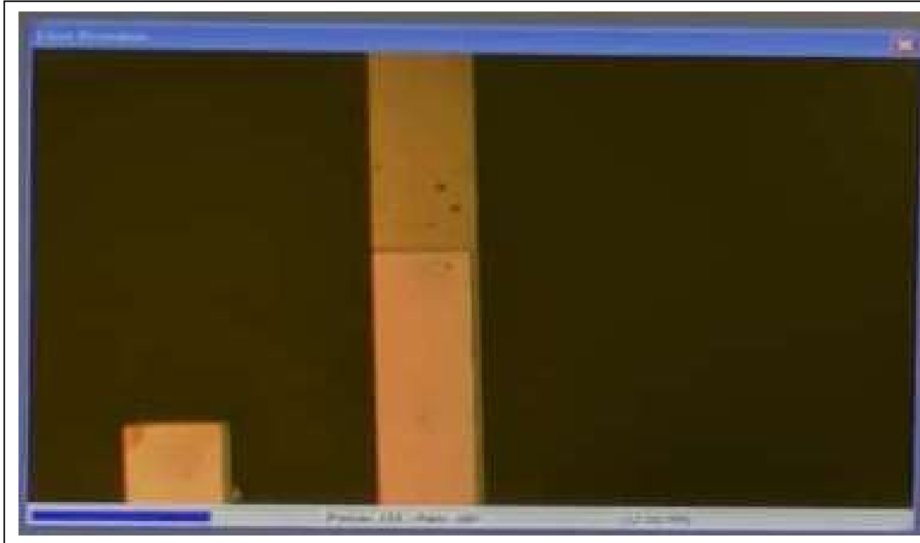



**Figure 9:** You can visibly see that the platinum metal parts of the wafers are a different color following PECVD than they were before. The color went from a more silver color before PECVD to a yellowish color following PECVD. This indicates that the deposition of $SiO_2$ was successful. Also, the locations (1 to 5) where oxide thickness was measured are labeled above.

**Table 2: Oxide Thickness at Different Locations**

| | **Wafer 1 Thickness (nm)** | **Wafer 2 Thickness** |
|---|---|---|
| **Location 1** | 241.6 | 249.1 |
| **Location 2** | 243.9 | 257.1 |
| **Location 3** | 241.7 | 249.0 |
| **Location 4** | 243.0 | 249.1 |
| **Location 5** | 241.9 | 249.5 |
| **Average** | 242.42 | 250.76 |
| **Standard Deviation** | 0.998 | 3.549 |

|  | **Figure 10:** The microscope image above very clearly shows the new feature. The lightest orange color is the newly deposited photoresist, while the more red part is where the previous photolithography step was. They are very closely aligned |
|---|---|

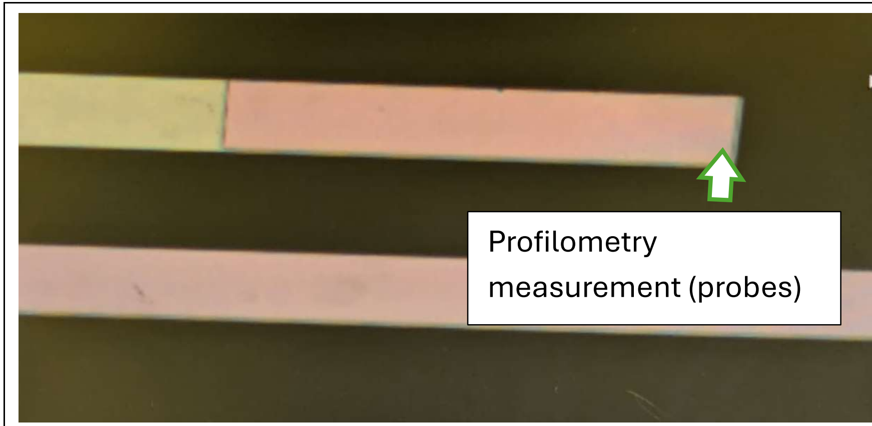
|   | **Figure 11:** In this microscope image following etching, profilometry images were taken at the end of the probes. |
|---|---|

**Table 3:**

| | Soldering Pads | Probes |
|---|---|---|
| Thickness | 0.234 µm | 0.234 µm |

## 3.4 Chip Assembly

Final chip assembly was successful and involved the laser-etching of holes, dicing of wafers, and soldering of wires.

The laser-etching step resulted in wafers with 4 holes of the correct size, passing fully through the wafer. No issues were encountered in this step, and it took 12 runs of the machine to fully cut through each wafer. A photograph of a wafer with finished holes can be seen in Figure 12.

No process issues were encountered during the dicing step. The wafers were diced into two halves along the centerline, as can be seen in Figure 13.

The soldering of wires to the devices was delayed by the stripping of the wires, which were small and hard to strip. Once soldering was complete, it resulted in connections that were visually effective as can be seen in Figure 14.

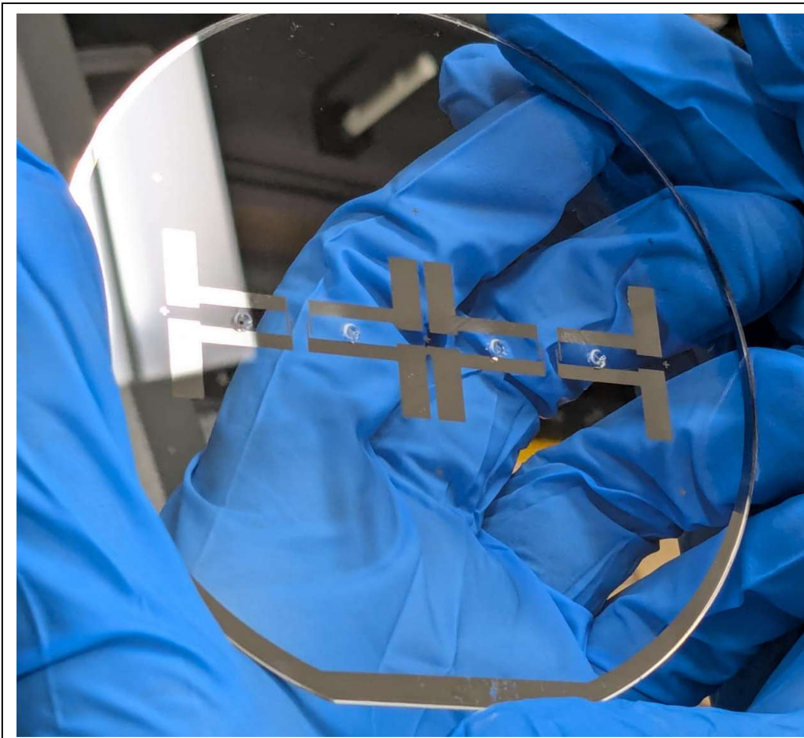


**Figure 12:** This is a photograph of the flow chip with the etched holes

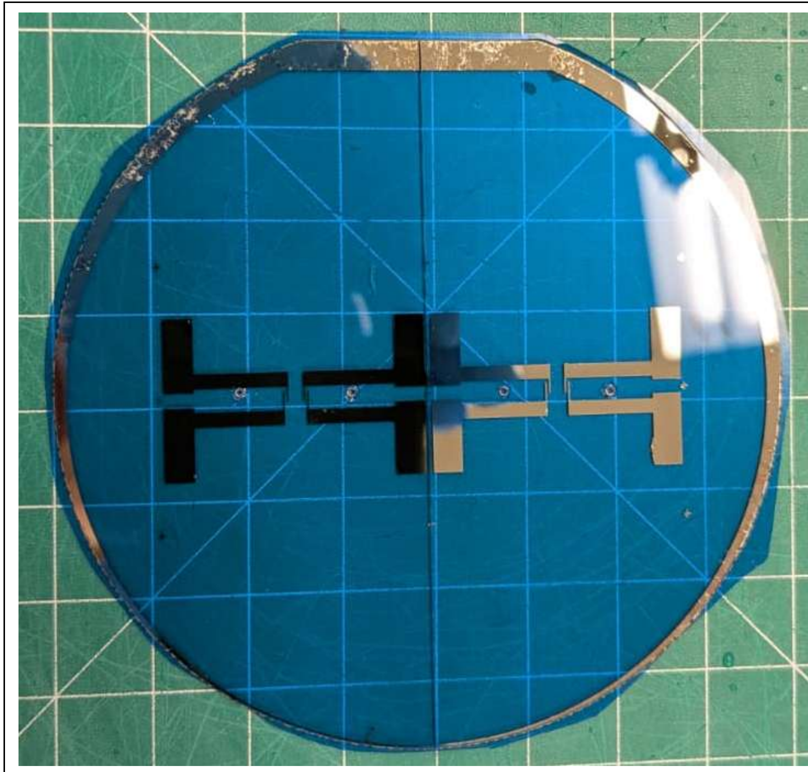


**Figure 13:** Camera photo of the diced chip

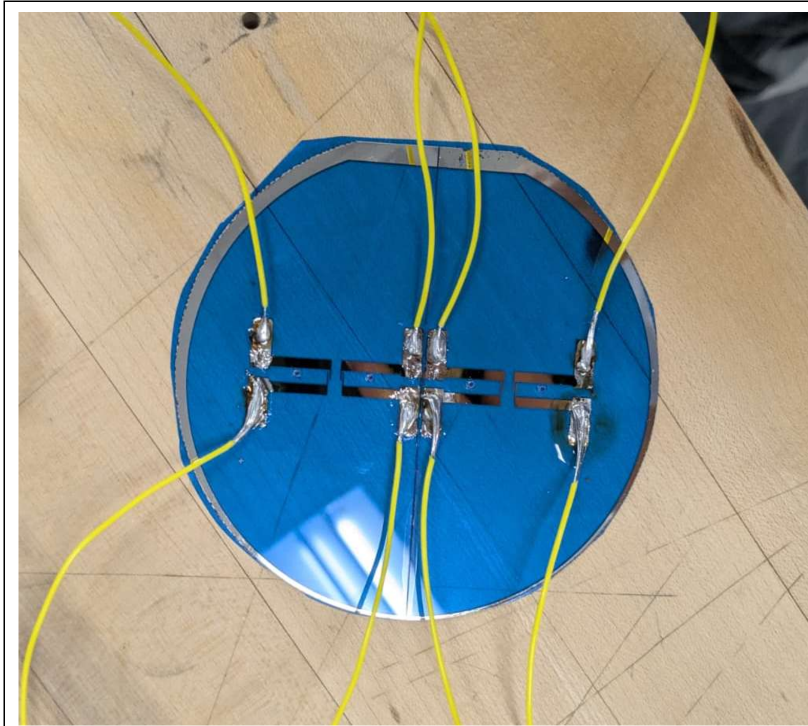


**Figure 14:** Camera photo of the soldered device

3.5 Testing

The electrolyte conductivity measurements performed in Lab 10 were successful, proving the effectiveness of the devices. For our lab section, 6 measurements were done for each different solution, and each of the measurements was performed by a different device. The results were inconsistent when comparing different devices to each other, but consistent for a single device. This consistency can be seen in Figure 15 below, where a linear fit was obtained with an $R^2$ value of 0.99. The cell constant value K was described by the following equation: K = 6.41 $m^{-1}$.

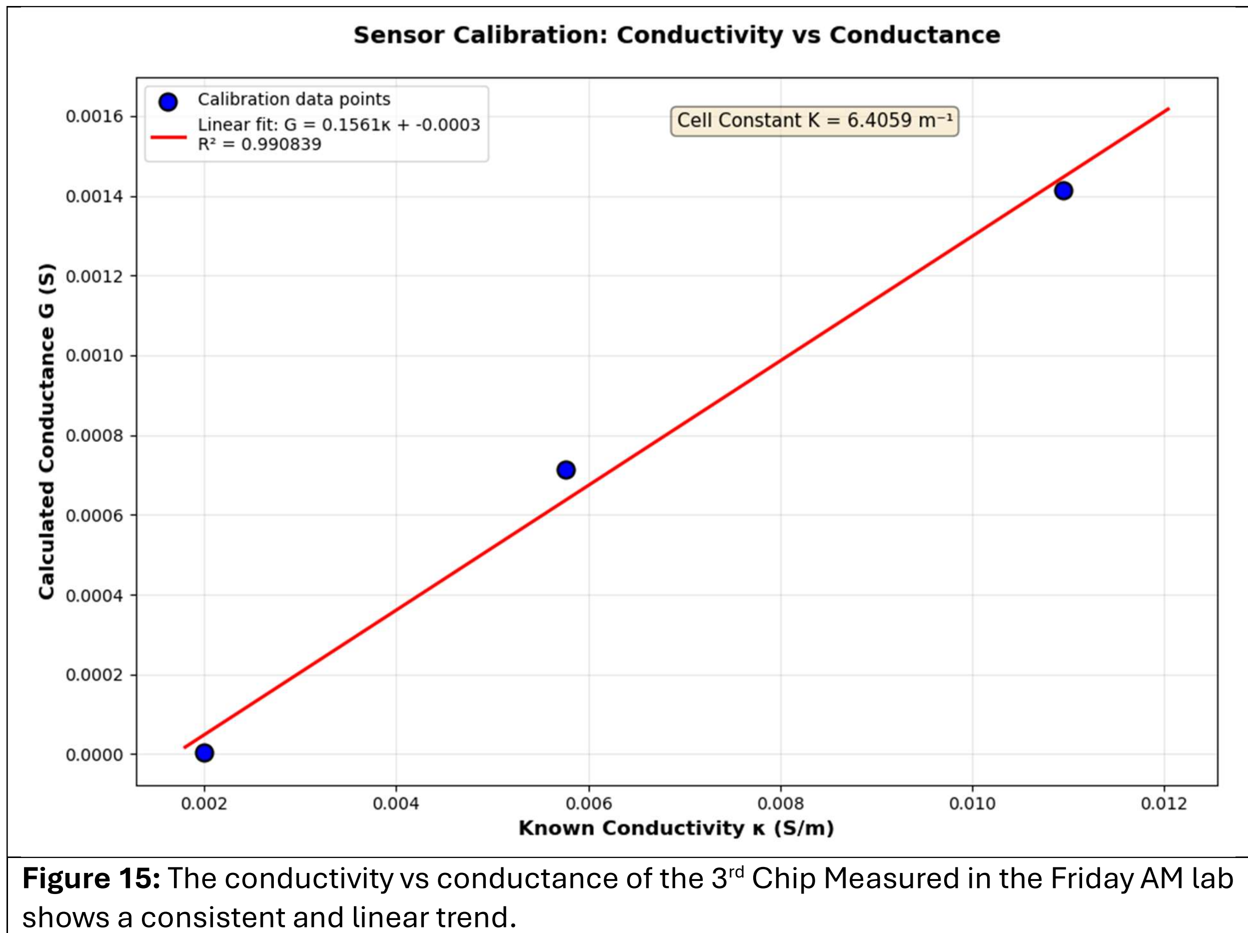



**Figure 15:** The conductivity vs conductance of the 3rd Chip Measured in the Friday AM lab shows a consistent and linear trend.

## 4. Conclusion

The outcomes of our labs were very positive, as there were few errors through the various processes and the resulting devices were functional. The wafers were generally good, except for an electrical shorting error that was caused by a damaged mask during lithography. This error meant that, once the wafers were diced in half, one half of each wafer was functional while the other half was not.

The fabrication process was effective, however some improvements could be made to make it easier in the future. The first mask, which was used for the metal patterning step, should be redesigned to decrease the risk of failed wafers. The soldering pads should be moved further apart to reduce the risk of electrical shorts.

Something I really enjoyed learning in the lab was the photolithography process. I found this process interesting because there were so many different steps to complete, and it was a very active process. I also enjoyed the wet etch process as well.

## 5. Acknowledgements

We would like to thank the University of Utah Nanofab staff, Professor Roseanne Warren, and the Porter Lab at BYU for their various contributions to this project. We would also like to thank our lab TA Vincent Banh, for leading us through the micromachining steps and helping deal with technical issues as they arose in the process.